IN THE SPECIFICATION

Please replace the paragraph beginning at line 1 on Page 6 with the following paragraph:

-- Referring to the drawings more particularly by reference numbers, FIGS. 3 and 4 shows a ball grid array ("BGA") integrated circuit package 10 of the present invention. The package 10 includes a substrate 12 that has a top surface 14 and an opposite bottom surface 16. Mounted to the top surface 14 of the substrate 12 is an integrated circuit [[16]] 18. The integrated circuit 18 is typically a microprocessor. Although a microprocessor is described, it is to be understood that the package 10 may contain any electrical device(s). --

Please replace the paragraph beginning at line 13 on Page 6 with the following paragraph:

-- The top surface 14 of the substrate 12 has a plurality of bond pads 20 and a ground bus 22. The substrate 12 may also have a separate power bus 23 concentrically located about the integrated circuit 18 and ground pad 22. The integrated circuit 18 is coupled to the bond pads 20 and busses 22 and 23 by bond wires 24. The integrated circuit [[16]] 18 is typically enclosed by an encapsulant 26. Although bond wires 24 are shown and described, the integrated circuit 18 can be mounted and coupled to the substrate with solder balls located on the bottom surface of the circuit die in a package and process commonly referred to

as "C4" or "flip chip" packaging. - -

Please replace the paragraph beginning at line 9 on Page 7 with the following paragraph:

- - The contact pads 28 are arranged in an outer two-dimensional array 36 and a center two-dimensional array 38. Each array contains a plurality of contact pads 28 that are separated from each other by a number of dielectric spaces 40. The outer array 36 is separated from the center array 38 by a dielectric area 42. The outer array [[38]] 36 is preferably located outside of the outer dimensional profile of the integrated circuit 18. In this manner the solder joints of the outer array [[38]] 36 are not subjected to stresses created by the difference in the coefficient of thermal expansion of the integrated circuit 18 and the expansion coefficient of the substrate 12. The center array 38 is located near the origin of the integrated circuit [[16]] 18 in an area that does not undergo as much thermal expansion as the outer edges of the circuit die. Therefore the solder stresses created by the differential thermal expansion is minimal in the area of the center array 38. The separated arrays provide a pattern that minimizes the stresses on the solder joints. - -

Please replace the paragraph beginning at line 1 on Page 8 with the following paragraph:

-- The outer array 36 is typically coupled to the signal lines of the integrated circuit [[16]] 18. The center array 38 is preferably coupled to the ground bus [[20]] 22 and power bus 23 of the substrate 12. The vias 30 that couple the busses 22 and 23 to the center contact pads 38 provide a direct thermal path through the substrate. The direct path lowers the thermal impedance of the package 10 and the junction temperature of the integrated circuit 18. Additionally, the short electrical path lowers the self-inductance and reduces the switching noise of the integrated circuit 18. --

Please replace the paragraph beginning at line 24 on Page 8 with the following paragraph:

-- Figure 5 shows an alternate embodiment of a package 10' which has five or six rows of contact pads 28 in the outer array 36' of the substrate 12'. The additional pads 28 increase the input/output (I/O) of the package 10'. The outer array 36' is preferably outside the outer dimensional profile of the integrated circuit 18 to minimize the stresses on the solder joints. The package 10' may provide 324 contact pads 28 on a 27 by 27 mm substrate 10. The longer rows of the package [[60]] 10' provide the approximate I/O of a 35 by 35 mm package, within the footprint of a 27 by 27 mm package. --